Amendments to the Specification:

Replace the paragraph beginning on page 3, line 1 as follows:

--FIGS. 5A[[,]] and 5B[[,]] ~~and 5C~~ illustrate a flow chart of the first part of a test algorithm for the memory test circuit of FIG. 1;--

Replace the paragraph beginning on page 7, line 14 as follows:

--The multiplexers 206, 208, 210, 212, and 214 ~~202, 204, 206, 208, and 210~~ connect each of the memory devices 106 either to the external circuit or to one of the test collars 104 in response to the "TEST_ENABLE" signal. The multiplexer 206 ~~202~~ switches the memory input data bus 226 between the external input data bus 222 and the internal input data bus 224 in response to the "TEST_ENABLE" signal 120. The multiplexer 208 ~~204~~ switches the memory enable line 232 between the external enable line 228 and the internal enable line 230. The multiplexer 210 ~~206~~ switches the memory address bus 238 between the external address bus 234 and the internal address bus 236. The multiplexer 212 ~~208~~ switches the memory write enable line 242 between the external write enable line 240 and the "WRITE_ENABLE" line 128. The multiplexer 214 ~~210~~ switches the memory clock line 248 between the external clock line 244 and the test clock line 246. The test clock is generated on the "TEST_CLOCK" line 246 according to well known techniques by circuitry included in the memory test circuit 100.--

Replace the paragraph beginning on page 8, line 11 as follows:

--The data comparator 218 compares the output data 220 with the internal input data 224. If they are not identical, the data comparator 218 generates the "TEST_OUT" signal 219 with a false value. The internal enable signal 230 is also input to the data comparator 218 to avoid generating data errors when the memory device 106 is not enabled by the address comparator 216. The "TEST_OUT" signal 219 ~~218~~ from each of the collars 104 is ANDed by the AND gates 108 with the "MBIST_GO" signal 132 to generate the "TEST_IN" signal 134. If any of the "TEST_OUT" signals 219 ~~218~~ is zero, then the "TEST_IN" signal 134 is also set to zero, and the "MBIST_GO" signal 132 is latched to zero. The latches 110 latch the control signals "TEST_ENABLE" 120, "D" 122, "CLEAR" 124, "NEXT" 126, "WRITE_ENABLE" 128, "MOVE" 130, and "MBIST_GO" 132 in response to the "TEST_ENABLE" signal 120 and the test clock signal 246 to locate a defective memory.--

Replace the paragraph beginning on page 11, line 7 as follows:

--FIGS. 5A[[,]] and 5B[[,]] ~~and 5C~~ illustrate a flow chart 500 of the first part of the test algorithm for the memory test circuit of FIG. 1. Logic operations are indicated in capital letters, for example, "A OR B" means "A logically OR'ed with B". The logic operations used are OR, XOR (exclusive OR), AND, and NOT. Also, the values of one and zero associated with the logic operations are used herein including the claims only to indicate one of two logical states (true or false) and have no numerical significance.--